Institute of Engineering
JIWAJI UNIVERSITY

PRESENTATION
ON
TV & RADAR

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EL- 804

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ASPECTRATIO

The ratio between width to height of rectangle picture frame adopted in TV system is known as aspect ratio.

Aspect ratio = Width/ Height = 4/ 3 or 4: 3

Reasons for having this ratio is

- Most of the objects are moving only in horizontal plane and so a larger width is desirable.
- Our eye can see the movement of object comfortably only in horizontal plane than in vertical plane.
- The frame size of motion picture already existing is having the aspect ratio of 4 : 3

PERSISTANCE OF VISION&FLICKER

- The sensation produced by incident light on the nerves of the eyes retina does not cease immediately. It persists for about 1/25th of a second (.062 Sec.) This storage characteristic is called as persistence of vision of eye.

- Flicker means if the scanning rate of picture is low, the time taken to move one frame to another frame will be high. This results in alternate bright and dark picture in the screen. This is called “Flicker”.

- To avoid flicker, the scanning rate of the picture should be increased i.e. 50 frames/Sec.

HORIZONTAL AND VERTICAL RESOLUTION

The ability of the image reproducing system to resolve the fine details of the picture distinctly in both horizontal and vertical direction is called as "resolution".

VERTICAL RESOLUTION:

The ability to resolve and reproduce fine details of picture in vertical direction is called as Vertical resolution.

$$Vr = Na \times k$$

where *Vr is the vertical resolution expressed in number of lines*

Na is the active number of lines

k is the resolution factor (also known as Kell factor)

Assuming a reasonable value of $k = 0.69$,

$$Vr = 585 \times 0.69 = 400 \text{ lines}$$

HORIZONTAL RESOLUTION :

The ability of the system to resolve maximum number of picture elements along the scanning determines the horizontal resolution.

$$Na \times aspect\ ratio = 585 \times 4/3 = 780$$

Therefore, the effective number of alternate black and white segments in one horizontal line for equal vertical and horizontal resolution are

$$N = Na \times aspect\ ratio \times k = 585 \times 4/3 \times 0.69 = 533$$

To resolve these 533 squares or picture elements the scanning spot must develop a video signal of square wave nature switching continuously
Since along one line there are $533/2 \approx 267$ complete cyclic changes, 267 complete square wave cycles get

VIDEO BANDWIDTH

Video Bandwidth = One horizontal line signal /One horizontal line tracing

= 267 /52 *10-6 = 5 MHz

Video Bandwidth = Horizontal Resolution /2* One Horizontal line scan

= 533/2*52 *10-6
= 5 MHz

COMPOSITE VIDEO SIGNAL (CVS)

CVS consists of

- Camera signal corresponding to the picture to be transmitted.
- Blanking pulses to made the retrace invisible.
- Sync pulse to synchronize the transmitter and receiver.

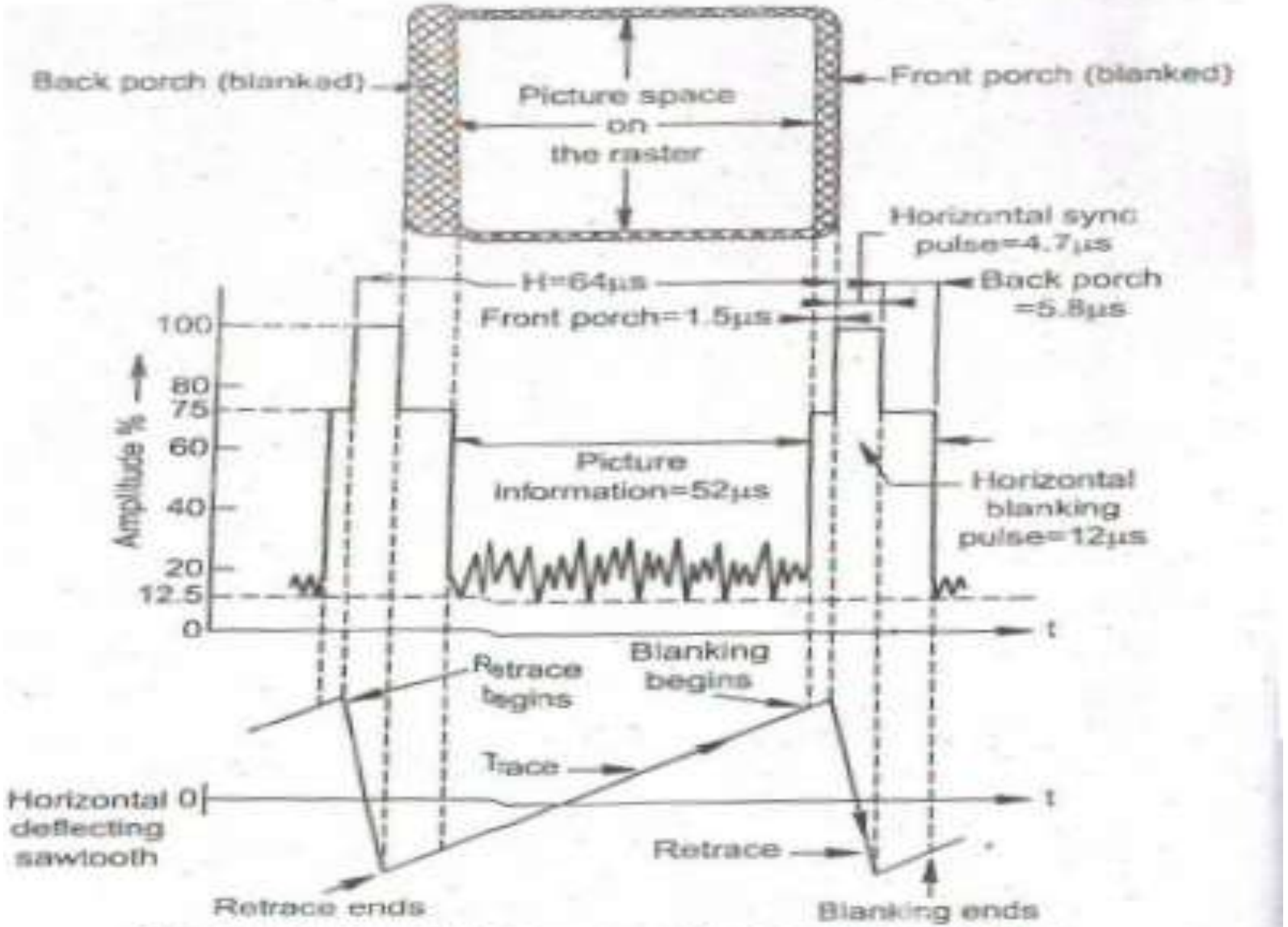


Fig.1.11 Composite video signal for one horizontal line

Details, Total amplitude is 100%
Y- axis Amplitude:

Extreme White level = 10%
Tolerance ± 2.5%
Black level = 70 % amplitude. Blanking retrace period amplitude increase to 70 %. But actually, blanking pulse of amp 75 % used
Blanking Pulse = 75% amplitude
Sync Pulse = 75% to 100% amplitude
X- axis Time details
Horizontal tracing time = 52 v Sec.
Horizontal retracing time = 12 v Sec.
H – Sync pulse time = 4.7 v Sec.

Difference between black level and blanking level is called as Pedestal. Average value of video signal is DC component. Distance between DC Component and pedestal is called as pedestal height.

FRONT PORCH:

Rising edge of sync pulse and blanking does not coincide. The time difference between the raising edge of sync and blanking pulse is called as ‘Front Porch”. It is 1.5 vs, ± .34 is tolerance. If front porch is not their sync. Pulse is build at varying fixed level and varying brightness level.

BACK PORCH:

Difference between the failing edge of sync pulse and blanking pulse is called back porch.

1. It allows horizontal fly back.
2. Used as reference level to preserve DC component.
3. Used to send colour burst signal in colour Transmission.
4. Used as AGC reference level in receiver circuits.

VERTICAL SEPRATED SYNC PULSE:

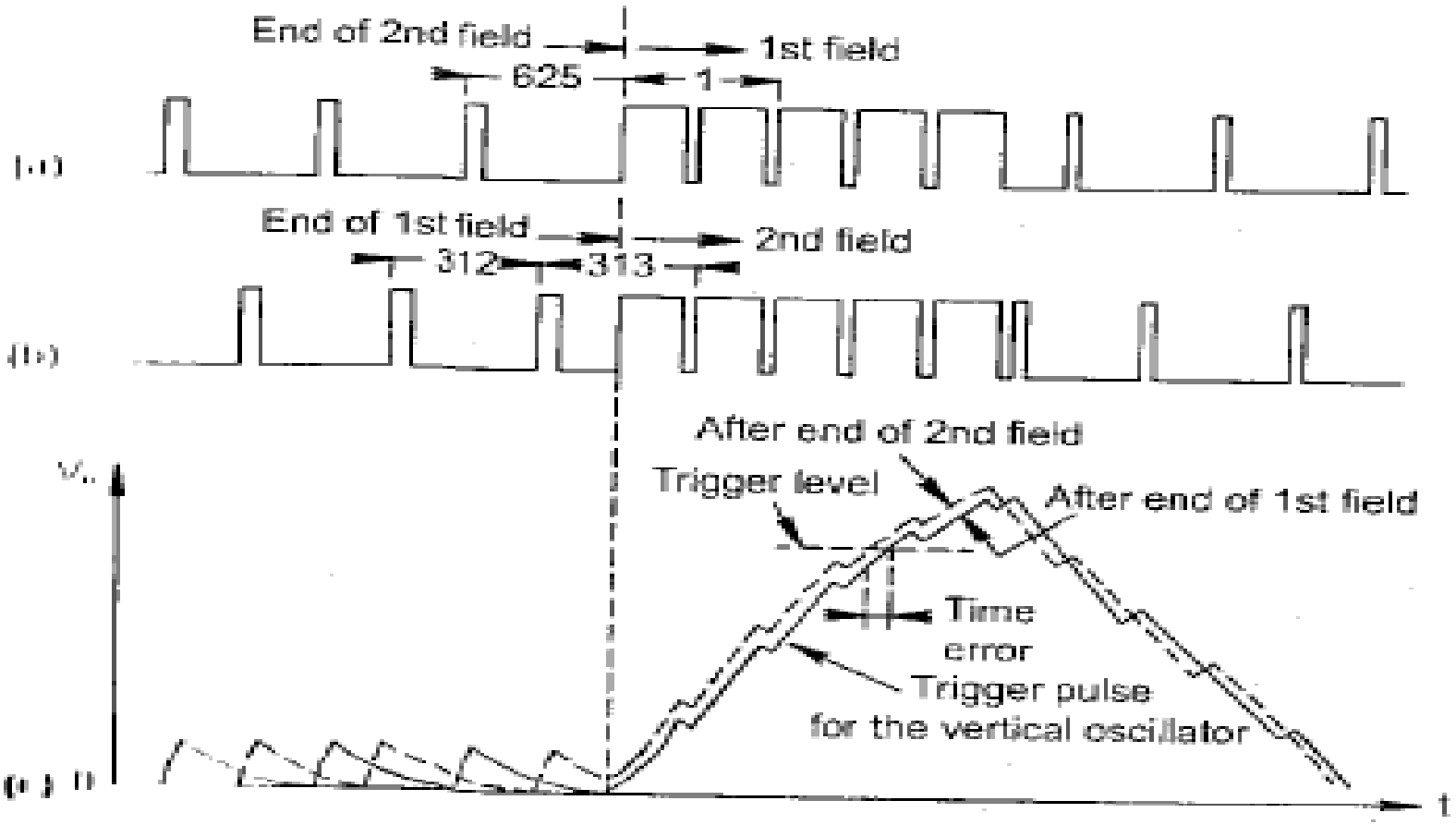


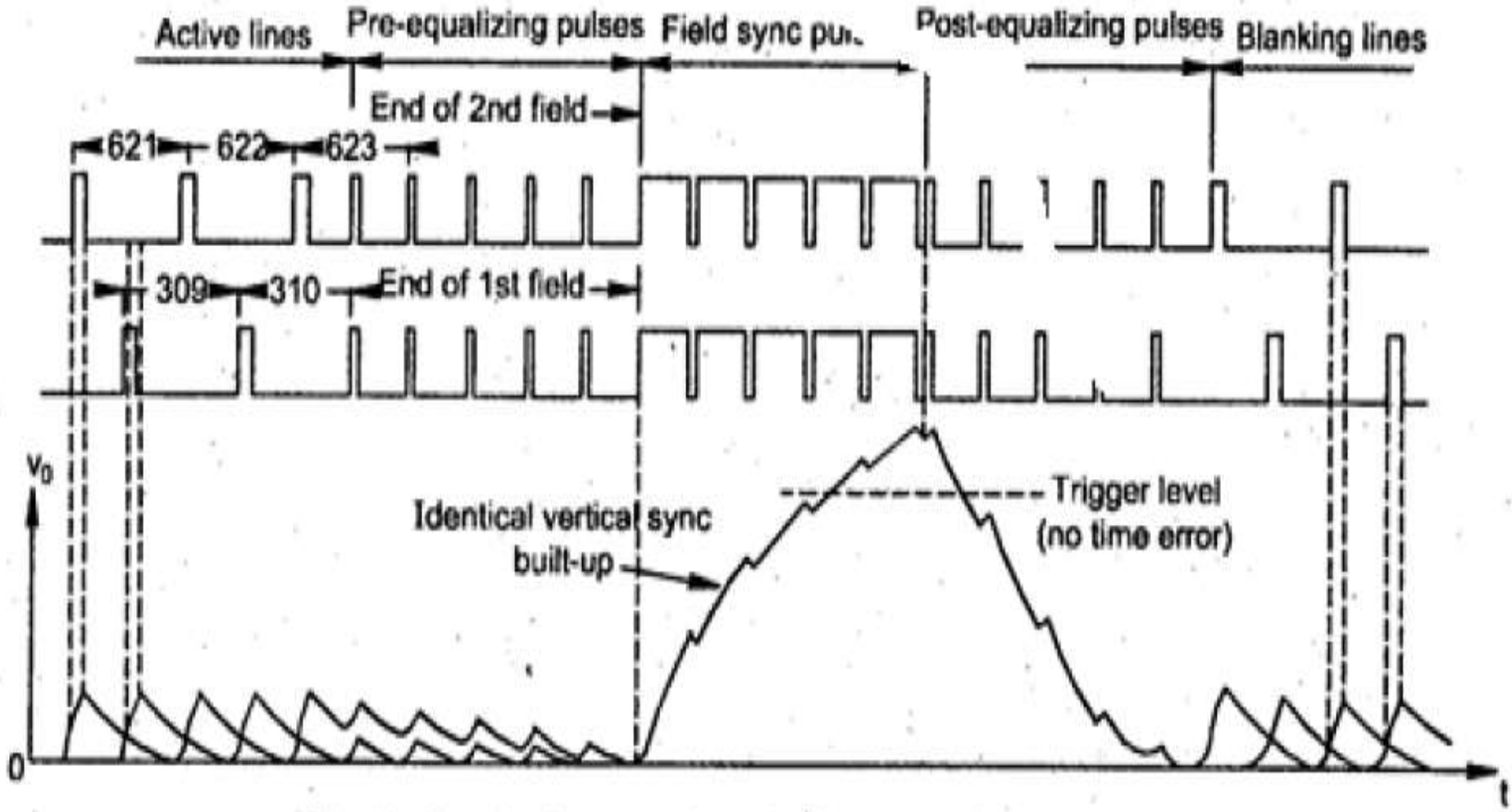
Fig. 1.12 Integrating waveforms (a) pulses at the end of 2nd (even) field (b) pulses at the end of 1st (odd) field (c) integrator output.

Here, vertical sync pulse of duration 160 s is divided into 5 pulses of duration 32 that too 4.7 on and 27.3 OFF period. This process is called as “serration”. This 4.7 sON is separated to have horizontal synchronization and it is given to differentiator the serrated pulses are given to integrator to get it as a single sync pulse. But here for odd and even fields their occurs time error due to trigger level in both fields. Because of charging and discharging of capacitor in the integrator. The time error due to trigger level of fields is called as “Half line discrepancy” occurs. To avoid half line discrepancy we are adding the equalizing pulses. Time error is because for second field in capacitor residual potential is zero. But for odd field, charging occurs of first field i.e., 312.5 lines. So there is some residual voltage and half line discrepancy occurs.

EQUALISING PULSES:

To avoid half line discrepancy due to time error in trigger level, equalizing pulses are used. These pulses are having duration of 2.3 vsec ON period and 27.4 vsec OFF period. Due to these pulses time error is completely avoided. The pulses added before the vertical sync pulse are called as “pre-equalising pulse and that added after the vertical sync pulses are called as post equalising pulses. Since the pulses are having a short duration 2.3 vsec the capacitor is charged to only small value. So before the start of vertical sync, during both field the capacitor is discharged to zero level.

Similarly due to post-equalising pulses this capacitor is discharged quickly. If the discharge is slow than the trailing edge, of integrator may false trigger the oscillator. The structure of pre and post equalising pulses are shown.



Identical vertical sync voltage built-up across the integrating capacitor

THANK YOU